芯片ESD测试 HBM测试 静电放电抗扰度试验等级 第三方检测机构

产品名称	芯片ESD测试 HBM测试 静电放电抗扰度试验等级 第三方检测机构
公司名称	质海检测技术（深圳）有限公司
价格	.00/件
规格参数	品牌:QTL质海检测 检测认证:第三方检测机构 服务类型:检测报告，检测认证
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产品详情

AEC_Q100-002中关于HBM测试的特殊要求：

一，测试电压要求，测试过程中不允许跳过电压进行测试

3.1 AEC HBM qualification testing shall be done at the following levels and skipping voltage levels is not allowed:

a. 500 V, 1000 V and 2000 V（加电压按照500V一个step进行加）

b. If failures are observed at 500 V, HBM testing at 250 V shall be done. If failures are observed at 250 V, HBM testing at 125 V shall be done. If the device fails at 250 V and a tester that meets waveform requirements at 125 V is not available, the part shall be classified Class 0A (i.e., < 125 V).

c. Voltage levels above 2000V may be done for margin, higher threshold targets or high robustness characterization.（大于2000V也需要测试一下窗口有多大）

二， Pin Stress Combinations

4.1 Devices with six (6) pins or less shall be tested with all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

4.2 HBM stress for AEC Q100 qualification shall be initially done using JS-001 Table 2B, with the following exceptions:

a. HBM stress using a Low Parasitic Tester (LPT) (see Section 4.3 below)

b. If a tester artifact is deemed to cause a false HBM failure, options contained within JS-001 Table 2A may be used. （tester的原因导致的fail，也可以转化为table 2A）

c. If a failure is deemed to be caused by cumulative stress, options contained within JS-001 Table 2A may be used. （如果累积fail出现，可以转化为table 2A）

4.3 AEC Q100 stress using a Low Parasitic Tester (LPT), such as a Two Pin HBM Tester.

a. Connectivity for each stress combination shall be verified. Refer to JS-001 Section 5.6.2 (“ Non Relay Testers ”).

b. Stress may use the Non-Supply to Non-Supply stress method found in JS-001 Table 2A (i.e., Pin combination N+1).

c. In addition to the Coupled Non-Supply Pin Pairs, adjacent Non-Supply pins on the die shall be stressed in two-pin mode.

d. Options outlined in JS-001 Section 6.6 (“ HBM Stressing with a Low Parasitic Simulator ”) related to LPT HBM testers may be used.